REMARKS

I. Introduction

By the present Amendment, claims 1, 6, and 11 have been amended. No claims have been added or canceled. Accordingly, claims 1-14 remain pending in the application. Claims 1, 6, and 11 are independent.

Applicants would like to thank Examiner Liang for the courtesy and cooperation extended during the interview conducted on October 3, 2006.

II. Office Action Summary

In the Office Action of April 4, 2006, claims 1 – 14 were rejected under 35 USC §102(e) as being anticipated by U.S. Patent No. 6,509,692 issued to Komiya. These rejections are respectfully traversed.

III. Rejections under 35 USC §102

The Office Action alleges that Komiya discloses an image display apparatus that comprises all the features recited in, for example, independent claim 1. More particularly, the Office Action indicates that Komiya provides a plurality of scanning wires, a plurality of signal wires, a plurality of current driven electro-optical display elements that are arranged in pixel regions surrounded by the scanning wires and the signal wires, and connected to a common power supply. The Office Action also indicates that Komiya discloses a plurality of driving elements arranged in the pixel region connected with the display elements. Further, the Office Action alleges that Komiya discloses memory control circuits that sample and hold the signal voltage while blocking a bias voltage from being applied to each of the driving elements. Subsequently, the memory control circuit allegedly applies the held voltage to the driving elements as the bias voltage. Applicants respectfully disagree.

As amended, independent claim 1 defines an image display apparatus that comprises:

> a plurality of scanning wires arranged in an image display region for transmitting a scanning signal;
>
> a plurality of signal wires arranged to intersect with said plurality of scanning wires in said image display region for transmitting a signal voltage;
>
> a plurality of current driven electro-optical display elements each arranged in a pixel region surrounded by said scanning wires and said signal wires connected to a common power supply;
>
> a plurality of driving elements arranged in said pixel region connected with said electro-optical display elements; and
>
> a plurality of memory control circuits each including a sampling switch and a driving switch for holding said signal voltage in response to said scanning signal and to control driving of said driving elements based on said held signal voltage,
>
> wherein said memory control circuit samples and holds said signal voltage while blocking a bias voltage from being applied to each of said driving elements by closing said sampling switch and opening said driving switch, and subsequently applies said held voltage signal to said driving elements as said bias voltage by opening said sampling switch and closing said driving switch.

According to independent claim 1, the image display apparatus comprises a plurality of scanning wires, a plurality of signal wires, a plurality of current driven opto-electrical display elements, a plurality of driving elements, and a plurality of memory control circuits. The plurality of scanning lines are arranged in an image display region for transmitting a scanning signal, while the plurality of signal lines are arranged to intersect the scanning wires in the image display region for transmitting a signal voltage. The current driven electro-optical display elements are each arranged in a pixel region surrounded by the scanning wires and signal wires, and connected to a common power supply. The driving elements are also arranged in the pixel region and connected to the electro-optical display elements. The memory

control circuits hold the signal voltage in response to the scanning signal in order to control driving of the driving elements based on the held signal voltage.

According to independent claim 1, each memory control circuit includes a sampling switch and a driving switch. The memory control circuit samples and holds the signal voltage while blocking a bias voltage from being applied to each of the driving elements. This is accomplished, in part, by closing the sampling switch and opening the driving switch during the sampling period. Subsequently, the memory control circuit applies the signal voltage being held to the driving elements as the bias voltage. This is accomplished by opening the sampling switch and closing the driving switch so that the signal voltage being held can be applied to the driving elements. See Fig. 4 and corresponding description.

Applicants' review of Komiya has failed to reveal any disclosure for the features recited in independent claim 1. Komiya discloses a self-emissive display device that includes a selection TFT having a control gate connected to a control line and a drain connected to a data line. A driving TFT is also provided with a gate connected to a source of the selection TFT. Komiya does not appear to disclose a display device capable of blocking the bias voltage during the sampling period. The configuration disclosed by Komiya is intended to apply a negative shift voltage V_{shift} to the cathode of the organic EL emissive element. See column 6, lines 5 – 17. Additionally, the memory control circuits of Komiya provide a storage capacitor that is directly connected to the control gate of the TFT. Consequently, it is not possible to isolate the voltage from the storage capacitor. See Fig. 7. Komiya fails to provide any disclosure for features presently recited in independent claim 1 such as:

> a plurality of memory control circuits each including a sampling switch and a driving switch for holding said signal voltage

in response to said scanning signal and to control driving of said driving elements based on said held signal voltage,

wherein said memory control circuit samples and holds said signal voltage while blocking a bias voltage from being applied to each of said driving elements by closing said sampling switch and opening said driving switch, and subsequently applies said held voltage signal to said driving elements as said bias voltage by opening said sampling switch and closing said driving switch.

It is therefore respectfully submitted that independent claim 1 is allowable over the art of record.

Claims 2 – 5 depend from independent claim 1, and are therefore believed allowable for at least the reasons set forth above with respect to independent claim 1. In addition, these claims each introduce novel elements that independently render them patentable over the art of record.

As Amended, Independent claim 6 defines an image display apparatus that comprises:

a plurality of scanning wires arranged in an image display region for transmitting a scanning signal;

a plurality of signal wires arranged to intersect with said plurality of scanning wires in said image display region for transmitting a signal voltage;

a plurality of current driven electro-optical display elements arranged in a pixel region surrounded by said scanning wires and said signal wires connected to a common power supply;

a plurality of driving elements arranged in said pixel region connected with said electro-optical display elements; and

a plurality of memory control circuits each including a sampling switch and a driving switch for holding said signal voltage in response to said scanning signal and to control driving of said driving elements based on said held signal voltage,

wherein said memory control circuit samples and holds said signal voltage in said sampling period by closing said sampling switch and opening said driving switch; and

wherein a voltage applied to said driving elements in a sampling period is lower than a voltage in a write period.

The image display apparatus of independent claim 6 provides a plurality of scanning wires that are arranged in an image display region for transmitting a scanning signal. A plurality of signal wires are also arranged to intersect with the scanning wires and to transmit a signal voltage. A plurality of current driven electro-optical display elements are arranged in pixel regions surrounded by the scanning wires and signal wires. The electro-optical display elements are also connected to a common power supply, and a plurality of driving elements are arranged in the pixel regions connected with the electro-optical display elements. Similar to independent claim 1, independent claim 6 provides a plurality of memory control circuits for holding the signal voltage in response to a scanning signal and control driving of the driving elements based on the signal voltage being held. Further, each memory control circuit includes a sampling switch and a driving switch. The memory control circuit samples and holds the signal voltage during the sampling period by closing the sampling switch and opening the driving switch. Further, a voltage applied to the driving elements in a sampling period is lower than the voltage during the right period.

As previously discussed with respect to independent claim 1, Komiya does not provide a sampling switch and driving switch. Accordingly, it is not possible for Komiya to provide a memory control circuit capable of sampling and holding the voltage signal during the sampling period. Additionally, the structure of Komiya provides a storage capacitor that is directly connected to the control gate of the TFT. Komiya simply fails to provide any disclosure for features recited in independent claim 6 such as:

> a plurality of memory control circuits each including a sampling switch and a driving switch for holding said signal voltage

in response to said scanning signal and to control driving of said driving elements based on said held signal voltage,

wherein said memory control circuit samples and holds said signal voltage in said sampling period by closing said sampling switch and opening said driving switch; and

wherein a voltage applied to said driving elements in a sampling period is lower than a voltage in a write period.

It is therefore respectfully submitted that independent claim 6 is allowable over the art of record.

Claims 7 – 10 depend from independent claim 6, and are therefore believed allowable for at least the reasons set forth above with respect to independent claim 6. In addition, these claims each introduce novel elements that independently render them patentable over the art of record.

Independent claim 11 defines an image display apparatus that comprises:

a plurality of scanning wires arranged in an image display region for transmitting a scanning signal;

a plurality of signal wires arranged to intersect with said plurality of scanning wires in said image display region for transmitting a signal voltage;

a plurality of current driven electro-optical display elements arranged in a pixel region which is surrounded by said scanning wires and said signal wires connected to a common power supply;

a plurality of driving elements arranged in said pixel region connected with said electro-optical display elements;

a plurality of memory control circuits each including a sampling switch and a driving switch for holding said signal voltage in response to said scanning signal and to control driving of said driving elements based on said held signal voltage;

a power supply control element for controlling electric power supplied from said common power supply to said driving elements,

wherein said memory control circuit samples and holds said signal voltage in said sampling period by closing said sampling switch and opening said driving switch; and

the electric power supplied to said driving elements in a sampling period is lower than the electric power in a write period.

Independent claim 11 recites features that are somewhat similar to those recited in independent claim 6. For example, the memory control circuits each include a sampling switch and a driving switch. Additionally, the memory control circuit samples and holds the signal voltage during the sampling period by closing the sampling switch and opening the driving switch. As previously discussed with respect to independent claim 6, this particular feature is not disclosed by Komiya.

It is therefore respectfully submitted that independent claim 11 is allowable over the art of record.

Claims 12 – 14 depend from independent claim 11, and are therefore believed allowable for at least the reasons set forth above with respect to independent claim 11. In addition, these claims each introduce novel elements that independently render them patentable over the art of record.

IV. Conclusion

For the reasons stated above, it is respectfully submitted that all of the pending claims are now in condition for allowance. Therefore, the issuance of a Notice of Allowance is believed in order, and courteously solicited.

If the Examiner believes that there are any matters which can be resolved by way of either a personal or telephone interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

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AUTHORIZATION

Applicants request any shortage or excess in fees in connection with the filing of this paper, including extension of time fees, and for which no other form of payment is offered, be charged or credited to Deposit Account No. 01-2135 (Case: 500.41297CX1).

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP.

Leonid D. Thenor
Registration No. 39,397

1300 N. Seventeenth Street
Suite 1800
Arlington, Virginia 22209
Tel: 703-312-6600
Fax: 703-312-6666

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LDT/gjb